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10/816,264	03/31/2004	Issy Kipnis	42P17422	9836

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EXAMINER	
MANDALA, VICTOR A	
ART UNIT	PAPER NUMBER
2826	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/29/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/816,264	KIPNIS ET AL.	
	Examiner	Art Unit	
	Victor A. Mandala Jr.	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 October 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11,19-24 and 29-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *29-35* is/are allowed.

6)☒ Claim(s) *1,2,4-10 and 19-24* is/are rejected.

7)☒ Claim(s) *3 and 11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/29/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of group I in the reply filed on 10/16/06 is acknowledged.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 6 and 19-24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 6 and 19 recite a high-resistivity silicon substrate, where it is unclear for the examiner to determine the definition of high resistivity when the disclosure has not recited a reference point, which would enable one to determine the starting point of high resistivity.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 6, 8, and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 4,672,421 Lin.

3. Referring to claim 1, Lin teaches of an interconnect apparatus comprising: a silicon substrate, (Figure 1 #30 and Col. 4 Lines 8-9); contact pads, (Figure 1 #34 and Figure 3 #54 or 64), processed on the silicon substrate, (Figure 1 #30 and Col. 4 Lines 8-9), to connect to an integrated circuit (IC) die, (Figure 1 #20, 22, 24, 26, & 28 and Figure 3 #56 & 60); interconnections, (Figure 3 #52 & 66 and Col. 5 Lines 3-8), selectively interconnecting the contact pads, (Figure 1 #34 and Figure 3 #54 or 64), the interconnections, (Figure 3 #52 & 66 and Col. 5 Lines 3-8), processed on the silicon substrate, (Figure 1 #30 and Col. 4 Lines 8-9); and circuit elements, (Figure 1 #20, 22, 24, 26, & 28 and Figure 3 #56 & 60), processed on the silicon substrate, (Figure 1 #30 and Col. 4 Lines 8-9), with the same processing, (Initially, and with respect to claim 1, note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Fitzgerald, 205 USPQ 594, 596 (CCPA); In re Marosi et al., 218 USPQ 289 (CAFC); and most recently, In re Thorpe et al., 227 USPQ 964 (CAFC, 1985) all of which make it clear that it is the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that Applicant has burden of proof in such cases as the above case law makes clear. As to the grounds of rejection under section 103, see MPEP § 2113), as the contact pads, (Figure 1 #34 and Figure 3 #54 or 64), and the interconnections, (Figure 3 #52 & 66 and Col. 5 Lines 3-8), to interoperate with the IC die, (Figure 1 #20, 22, 24, 26, & 28 and Figure 3 #56 & 60).

4. Referring to claim 6, Lin teaches of an interconnect apparatus according to claim 1, wherein the silicon substrate comprises a high-resistivity silicon substrate, (Figure 1 #30 and Col. 4 Lines 8-9 and insofar as to understand from the 112 2nd paragraph rejection above).

5. Referring to claim 8, Lin teaches of an interconnect apparatus according to claim 1, wherein the circuit elements comprise an active circuit element, (Col. 4 Lines 6-7.

6. Referring to claim 9, Lin teaches of an interconnect apparatus according to claim 1, further comprising a cap, (Figure 1 #46 and Col. 4 Lines 8-9), processed onto the silicon substrate, (Figure 1 #30 and Col. 4 Lines 8-9), to hermetically isolate circuit elements on the silicon substrate, (Figure 1 #30 and Col. 4 Lines 8-9).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 4-9, and 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Application No. 2003/0020094 Shrauger.

7. Referring to claim 1, Shrauger teaches of an interconnect apparatus comprising: a silicon substrate, (Figure 1, 6, & 12 #1 and Paragraph 0030 Lines 3-6); contact pads, (Figure 1 #2), processed on the silicon substrate, (Figure 1, 6, & 12 #1 and Paragraph 0030 Lines 3-6), to connect to an integrated circuit (IC) die, (Figure 4 Labeled as MEMS die); interconnections, (Figure 1 #2 & 3 and Figure 12 labeled as electrical interconnections), selectively

interconnecting the contact pads, (Figure 1 #2), the interconnections, (Figure 1 #2 & 3 and Figure 12 labeled as electrical interconnections), processed on the silicon substrate, (Figure 1, 6, & 12 #1 and Paragraph 0030 Lines 3-6); and circuit elements, (Figure 4 Labeled as MEMS die "the other one that is not labeled as the IC die" and Figure 12 #15), processed on the silicon substrate, (Figure 1, 6, & 12 #1 and Paragraph 0030 Lines 3-6), with the same processing, (Initially, and with respect to claim 1, note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Fitzgerald, 205 USPQ 594, 596 (CCPA); In re Marosi et al., 218 USPQ 289 (CAFC); and most recently, In re Thorpe et al., 227 USPQ 964 (CAFC, 1985) all of which make it clear that it is the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that Applicant has burden of proof in such cases as the above case law makes clear. As to the grounds of rejection under section 103, see MPEP § 2113), as the contact pads, (Figure 1 #2), and the interconnections, (Figure 1 #2 & 3 and Figure 12 labeled as electrical interconnections), to interoperate with the IC die, (Figure 4 Labeled as MEMS die).

8. Referring to claim 2, Shrauger teaches of an interconnect apparatus according to claim 1, wherein the circuit elements comprise a micro electro-mechanical system (MEMS) device, (Figure 4 Labeled as MEMS die "the other one that is not labeled as the IC die").

9. Referring to claim 4, Shrauger teaches of an interconnect apparatus according to claim 2, wherein the MEMS device further includes an actuation circuit device, (Figure 4 Labeled as MEMS die "the other one that is not labeled as the IC die" and Paragraph 0014).

10. Referring to claim 5, Shrauger teaches of an interconnect apparatus according to claim 1, wherein the circuit elements comprise, a sensor circuit, (Figure 10 #14 Photodetector).

11. Referring to claim 6, Shrauger teaches of an interconnect apparatus according to claim 1, wherein the silicon substrate comprises a high-resistivity silicon substrate, (Figure 1, 6, & 12 #1 and Paragraph 0030 Lines 3-6 and insofar as to understand from the 112 2nd paragraph rejection above).

12. Referring to claim 7, Shrauger teaches of an interconnect apparatus according to claim 6, wherein the circuit elements comprise optical circuit components, (Figure 10 #14 Photodetector and Figure 12 #15 laser).

13. Referring to claim 8, Shrauger teaches of an interconnect apparatus according to claim 1, wherein the circuit elements comprise an active circuit element, (Figure 12 #15 laser).

14. Referring to claim 9, Shrauger teaches of an interconnect apparatus according to claim 1, further comprising a cap, (Figure 7 Labeled as C), processed onto the silicon substrate, (Figure 1, 6, & 12 #1 and Paragraph 0030 Lines 3-6), to hermetically isolate circuit elements on the silicon substrate, (Figure 1, 6, & 12 #1 and Paragraph 0030 Lines 3-6).

15. Referring to claim 19, Shrauger teaches of an integrated circuit chip having a circuit element, (Figures 10 & 11 #130, 131, & 120), on a substrate, (Figures 10 & 11 #102 which a substrate is a layer that supports and layers formed thereon), created with a first lithographic processing, (Initially, and with respect to claim 19 and the limitations of processing and

lithography, note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Fitzgerald, 205 USPQ 594, 596 (CCPA); In re Marosi et al., 218 USPQ 289 (CAFC); and most recently, In re Thorpe et al., 227 USPQ 964 (CAFC, 1985) all of which make it clear that it is the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that Applicant has burden of proof in such cases as the above case law makes clear. As to the grounds of rejection under section 103, see MPEP § 2113), interconnected on a high-resistivity silicon interconnect substrate, (Figure 10 & 11 #101 Paragraph 0069 Lines 10-11 and insofar as to understand from the 112 2nd paragraph rejection above), having functional circuit elements, (Figures 10 & 11 #150 & 152), embedded in the interconnect substrate, (Figure 10 & 11 #101), created by the process of: processing contact pads, (Figure 10 & 11 #221), and electrical traces, (Figure 10 & 11 #222), on the silicon substrate, (Figure 10 & 11 #101), with a second lithographic processing to interconnect the circuit elements, (Figures 10 & 11 #150 & 152); processing the circuit elements, (Figures 10 & 11 #130, 131, & 120), on the interconnection substrate, (Figures 10 & 11 #101), with the second lithographic processing; and interconnecting, (Figure 10 shows the driving and sensor circuits connected to the MEMS through layer #104), the circuit element, (Figures 10 & 11 #130, 131, & 120), of the first lithographic processing on the separate substrate, (Figures 10 & 11 #102 which

a substrate is a layer that supports and layers formed thereon), to contact pads, (Figures 10 & 11 #221), on the interconnection substrate, (Figures 10 & 11 #101).

16. Referring to claim 20, Shrauger teaches of an integrated circuit chip according to claim 19, wherein the silicon interconnect substrate further includes a micro electro-mechanical system (MEMS) device, (Figures 10 & 11 #130, 131, & 120).

17. Referring to claim 21, Shrauger teaches of an integrated circuit chip according to claim 19, wherein the circuit elements comprise an active circuit element, (Figure 10 labeled as Driving circuit).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 5-10, 19, 21, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Application No. 6,998,691 Baugh et al.

18. Referring to claim 1, Baugh et al. teaches of an interconnect apparatus comprising: a silicon substrate, (Figure 1 #120 and Col. 4 Line 14); contact pads, (Figure 1 #122), processed on the silicon substrate, (Figure 1 #120), to connect to an integrated circuit (IC) die, (Figure 1 #110); interconnections, (Figure 1 not shown, but Col. 4 Lines 17-18), selectively interconnecting the contact pads, (Figure 1 #122), the interconnections, (Figure 1 not shown, but

Col. 4 Lines 17-18), processed on the silicon substrate, (Figure 1 #120 and Col. 4 Line 14); and circuit elements, (Figure 1 not shown, but Col. 4 Lines 22-24), processed on the silicon substrate, (Figure 1 #120 and Col. 4 Line 14), with the same processing, (Initially, and with respect to claim 1, note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Fitzgerald, 205 USPQ 594, 596 (CCPA); In re Marosi et al., 218 USPQ 289 (CAFC); and most recently, In re Thorpe et al., 227 USPQ 964 (CAFC, 1985) all of which make it clear that it is the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that Applicant has burden of proof in such cases as the above case law makes clear. As to the grounds of rejection under section 103, see MPEP § 2113), as the contact pads, (Figure 1 #122), and the interconnections, (Figure 1 not shown, but Col. 4 Lines 17-18), to interoperate with the IC die, (Figure 1 #110).

19. Referring to claim 5, Baugh et al. teaches of an interconnect apparatus according to claim 1, wherein the circuit elements comprise, a sensor circuit, (Figure 1 not shown, but Col. 4 Lines 22-24).

20. Referring to claim 6, Baugh et al. teaches of an interconnect apparatus according to claim 1, wherein the silicon substrate comprises a high-resistivity silicon substrate, (Figure 1 #120 and Col. 4 Line 14 and insofar as to understand from the 112 2nd paragraph rejection above).

21. Referring to claim 7, Baugh et al. teaches of an interconnect apparatus according to claim 6, wherein the circuit elements comprise optical circuit components, (Figure 1 not shown, but Col. 4 Lines 22-24).

22. Referring to claim 8, Baugh et al. teaches of an interconnect apparatus according to claim 1, wherein the circuit elements comprise an active circuit element, (Figure 1 not shown, but Col. 4 Lines 22-24).

23. Referring to claim 9, Baugh et al. teaches of an interconnect apparatus according to claim 1, further comprising a cap, (Figure 1 #130), processed onto the silicon substrate, (Figure 1 #120 and Col. 4 Line 14), to hermetically isolate circuit elements on the silicon substrate, (Figure 1 #120 and Col. 4 Line 14).

24. Referring to claim 10, Baugh et al. teaches of an interconnect apparatus according to claim 9, wherein the cap comprises a cap of silicon-based material, (Figure 1 #130 and Col. 4 Lines 28).

25. Referring to claim 19, Baugh et al. teaches of an integrated circuit chip having a circuit element, (Figure 1 #110), on a substrate, (Figure 1 not labeled but the internal substrate of #110), created with a first lithographic processing, (Initially, and with respect to claim 19 and the limitations of processing and lithography, note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Fitzgerald, 205 USPQ 594, 596 (CCPA); In re Marosi et al., 218 USPQ 289 (CAFC); and most recently, In re Thorpe et al., 227 USPQ 964 (CAFC, 1985) all of which make it clear that it is the final product per se which must be

determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that Applicant has burden of proof in such cases as the above case law makes clear. As to the grounds of rejection under section 103, see MPEP § 2113), interconnected on a high-resistivity silicon interconnect substrate, (Figure 1 #120 and Col. 4 Line 14 and insofar as to understand from the 112 2nd paragraph rejection above), having functional circuit elements, (Figure 1 not shown, but Col. 4 Lines 22-24), embedded in the interconnect substrate, (Figure 1 #120 and Col. 4 Line 14), created by the process of: processing contact pads, (Figure 1 #122), and electrical traces, (Figure 1 not shown, but Col. 4 Lines 17-18), on the silicon substrate, (Figure 1 #120 and Col. 4 Line 14), with a second lithographic processing to interconnect the circuit elements, (Figure 1 not shown, but Col. 4 Lines 22-24); processing the circuit elements, (Figure 1 not shown, but Col. 4 Lines 22-24), on the interconnection substrate, (Figure 1 #120 and Col. 4 Line 14), with the second lithographic processing; and interconnecting, (Figure 1 not shown, but Col. 4 Lines 17-18), the circuit element, (Figure 1 #110), of the first lithographic processing on the separate substrate, (Figure 1 not labeled but the internal substrate of #110), to contact pads, (Figure 1 #122), on the interconnection substrate, (Figure 1 #120 and Col. 4 Line 14).

26. Referring to claim 21, Baugh et al. teaches of an integrated circuit chip according to claim 19, wherein the circuit elements comprise an active circuit element, (Figure 1 not shown, but Col. 4 Lines 22-24).

27. Referring to claim 23, Baugh et al. teaches of an integrated circuit chip according to claim 19, wherein the silicon interconnect substrate, (Figure 1 #120), further comprises a silicon

lid, (Figure 1 #130 and Col. 4 Lines 28), to hermetically seal functional circuit elements, (Figure 1 not shown, but Col. 4 Lines 22-24).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Application No. 6,998,691 Baugh et al. in view of U.S. Patent No. 6,420,197 Ishida et al.

28. Referring to claim 22, Baugh et al. in view of Ishida et al. teaches of an integrated circuit chip according to claim 19, wherein the circuit elements on separate substrates, (Baugh et al. Figure 1 #110, which are lasers Col. 4 Line 16), comprise circuit elements all on silicon substrates, (Baugh et al. is silent in regard to the laser being formed on a silicon substrate, but Ishida et al. does in Col. 1 Lines 17-20 and where it would have been obvious to one having ordinary skill in the art at the time the invention was made to make the laser on a silicon substrate because of the low cost and high availability, and since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.)

Allowable Subject Matter

29. Claim 3 and 11 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

30. Claim 24 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

31. Claims 29-35 are allowed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Victor A. Mandala Jr. whose telephone number is (571) 272-1918. The examiner can normally be reached on Monday through Thursday from 8am till 6pm..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

VAMJ
1/19/07

EVAN PERT
PRIMARY EXAMINER